CLAIMS

I claim:

1. A method comprising:

generating a first pixel stream on a first clock signal, the first clock signal being from a first source;

forwarding a second clock signal from a second source and the first pixel stream to a buffer to translate the first pixel stream into a second pixel stream on the second clock signal; and

providing a feedback to the second source to cause the second source to adjust the center frequency of the second clock signal to match the average frequency of the first clock signal with the average frequency of the second clock signal.

2. The method of claim 1, wherein providing a feedback comprises sending a signal from the buffer to the second source when the content of the buffer reaches a predetermined threshold value.

3. The method of claim 1, wherein providing a feedback comprises:

counting clock edges of the first clock signal on the first source;

counting clock edges of the second clock signal on the second source; and

sending a signal to the second source when the number of the clock edges on the first source is different from the number of the clock edges on the second source.

4. The method of claim 3, wherein the second source includes a phase lock loop.

5. The method of claim 1, wherein the first clock signal is a non-spread spectrum modulation clock signal and the second clock signal is a spread spectrum modulation clock signal.

6. The method of claim 1, further comprising:

forwarding the first pixel stream to a cathode ray tube ("CRT") display; and

forwarding the second pixel stream to a liquid crystal display ("LCD") panel.

7. An apparatus comprising:

a first circuitry to generate a first clock signal;

a display pipe being coupled to the first circuitry to receive the first clock signal and to generate a first pixel stream on the first clock signal;

a buffer being coupled to the display pipe to receive the first pixel stream and a second clock signal and to transform the first pixel stream into a second pixel stream on the second clock signal; and

a second circuitry being coupled to the buffer to generate the second clock signal and to receive a feedback, wherein the second circuitry adjusts the center frequency of the second clock signal in response to the feedback.

8. The apparatus of claim 7, wherein the buffer sends the feedback to the second circuitry when the buffer content reaches a predetermined threshold value.

9. The apparatus of claim 7 further comprising a counter being coupled to the first circuitry to count clock edges of the first clock signal and the second circuitry to count clock edges of the second clock signal, wherein the counter sends the feedback to the second circuitry when the number of clock edges of the first clock signal is different from the number of clock edges of the second clock signal.

10. The apparatus of claim 9, wherein the second circuitry comprises a phase lock loop.

11. The apparatus of claim 7, wherein the first clock signal is a non-spread spectrum modulation clock signal and the second clock signal is a spread spectrum modulation clock signal.

12. The apparatus of claim 7, wherein the first pixel stream is forwarded to a cathode ray tube ("CRT") display and the second pixel stream is forwarded to a liquid crystal display ("LCD") panel.

13. A system comprising:

a dynamic random access memory ("DRAM");

a graphic memory controller hub being coupled to the DRAM, the graphic memory controller hub comprising

a first circuitry to generate a first clock signal;

a display pipe being coupled to the first circuitry to receive the first clock signal and to generate a first pixel stream on the first clock signal;

a buffer being coupled to the display pipe to receive the first pixel stream and a second clock signal and to transform the first pixel stream into a second pixel stream on the second clock signal; and

a second circuitry being coupled to the buffer to generate the second clock signal and to receive a feedback, wherein the second circuitry adjusts the center frequency of the second clock signal in response to the feedback.

14. The system of claim 13, wherein the buffer sends the feedback to the second circuitry when the buffer content reaches a predetermined threshold value.

15. The system of claim 13, wherein the graphic memory controller hub further comprises a counter being coupled to the first circuitry to count clock edges of the first clock signal and the second circuitry to count clock edges of the second clock signal, and to send the feedback to the second circuitry when the number of clock edges of the first clock signal is different from the number of clock edges of the second clock signal.

16. The system of claim 15, wherein the second circuitry comprises a phase lock loop.

17. The system of claim 13, wherein the first clock signal is a non-spread spectrum modulation clock signal and the second clock signal is a spread spectrum modulation clock signal.

18. The system of claim 13 further comprising a liquid crystal display ("LCD") panel being coupled to the graphic memory controller hub to receive the second pixel stream.

19. The system of claim 18, wherein the first pixel stream is forwarded to a cathode ray tube ("CRT") display.

20. The system of claim 13 further comprising a processor being coupled to the graphic memory controller hub.